XD6132/33/34 High Performance Voltage Detectors

AEC-Q100 Grade 1

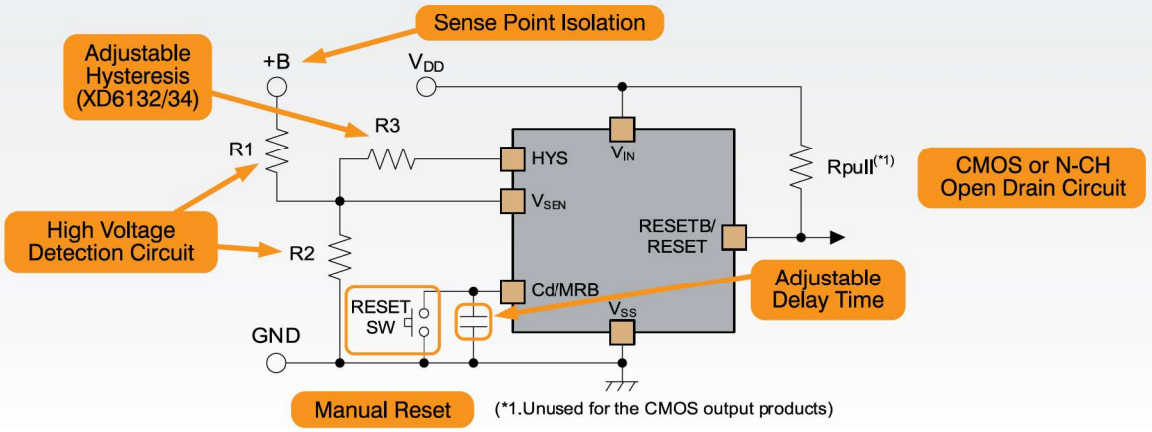
The XD6132/33/34 series are ultra-small voltage detectors that have high accuracy and sense pin for monitoring a rail other than VIN. High accuracy and low supply current are achieved by means of a low power, highly accurate internal reference in CMOS technology.

The sense pin is isolated from the power input pin to enable monitoring of the voltage of another power supply. Output can be maintained in the detection state even if the voltage of the power supply that is monitored drops to 0V. The sense pin is also suitable for detecting high voltages, and the detection and release voltage can be set as desired using an external resistance.

KEY FEATURES

SERIES	XD6132	XD6133	XD6134
Operating Voltage Range	1.6V ~ 6.0V		
Detect Voltage Range	0.8V ~ 2.0V	1.0V ~ 5.0V	0.8V ~ 5.0V
Detect Voltage Accuracy (-40°C ~ 125°C)	±2.7% (2.0V ≥ VDF ≥ 1.5V) ±36mV (VDF < 1.5V)	±2.7% (3.0V ≥ VDF ≥ 1.5V), ±3.0% (5.0V ≥ VDF ≥ 3.1V) ±36mV (VDF < 1.5V)	
Temp Characteristics	±50ppm/°C (Typ.)		
Output Configuration	CMOS or N-Channel Open Drain		
Output Logic	H level or L level at detection		
Power Consumption	1.28μA (at Detection), 1.65μA (at Release)		
Hysteresis width	VDF×0.1%(Typ.)	VDF×5% (Typ.)	VDF×0.1% (Typ.)
Additional Features	Adj. Hysteresis Width	–	Adj. Hysteresis Width
	Manual RESET		
	Delay Capacitance Pin		
	Release delay / detection delay can be set 4 time ratio patterns		
	Sense Pin with Surge Voltage Protection	Sense Pin	
Op. Ambient Temperature	-40°C ~ 125°C		
AEC-Q100	Grade 1		
Package	SOT-26, USP-6C		

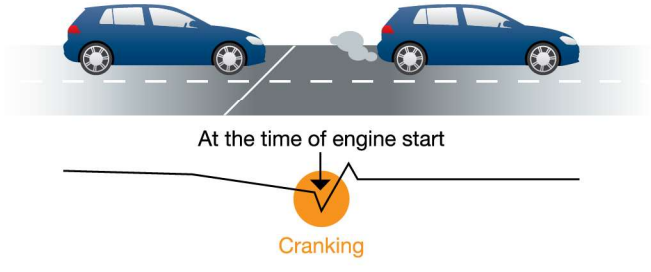
TYPICAL APPLICATION CIRCUIT

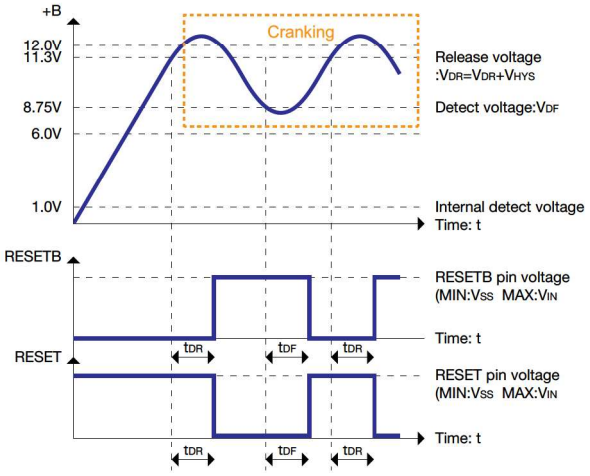


VEHICLE BATTERY DETECTION DURING CRANKING

Avoid False Detection during Cranking

- ✔ Adjustable V_{DR} and V_{DF} with resistor division
- ✔ Adjustable Hysteresis with only one external resistor
- ✔ Adjustable t_{DT} and t_{DR} with external capacitor

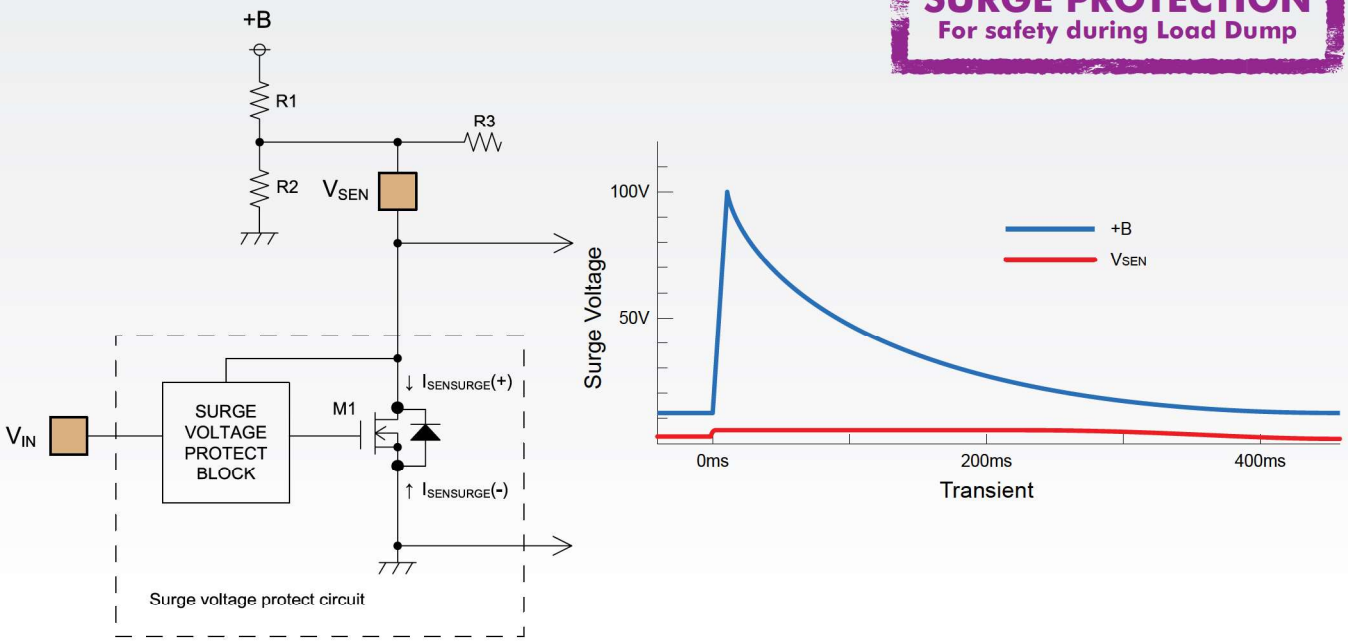




INTEGRATED LOAD DUMP PROTECTION

XD6132 SURGE VOLTAGE PROTECTION

SURGE PROTECTION
For safety during Load Dump



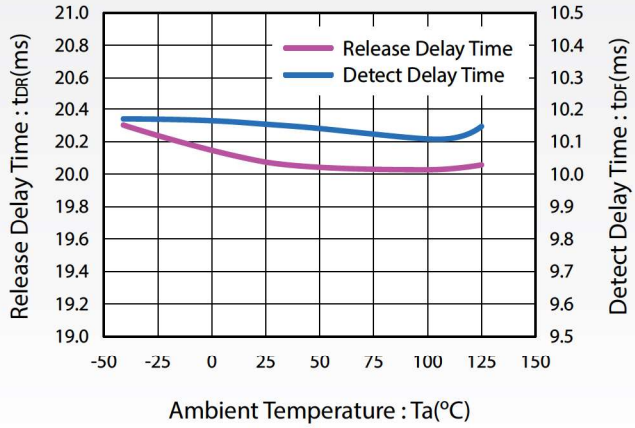
Even if 100V Load dump surge comes to +B, the internal surge voltage protection circuit protects the VSEN pin. When the surge comes and the VSEN voltage rises, the "SURGE VOLTAGE PROTECT BLOCK" detects it and turns on M1 which sinks 2.5mA and this current causes a voltage drop on R1 to keep VSEN safe.

EXCELLENT TEMPERATURE CHARACTERISTICS

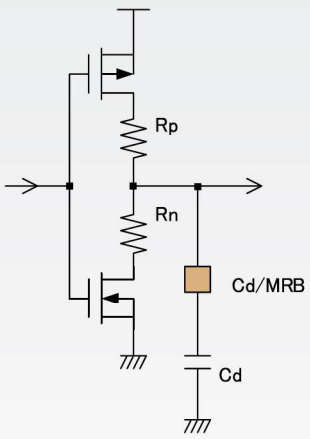
HIGH OPERATING TEMPERATURE

XD6132/XD6133/XD6134

V_{IN}=3.3V, V_{SEN}=0.9V⇔1.1V
Cd=0.1μF, Rp=288kΩ (t_{DR}=20ms)
Rn=144kΩ (t_{DF}=10ms)



RELEASE DELAY AND DETECTION DELAY COMBINATION



The release delay is set by Rp and Cd and the detect delay time is set by Rn and Cd. The release delay allows you to start up correctly and the detect delay avoids any mis-detection due to noise and spikes. The XD6132/33/34 has five (5) different ratio configurations of Rp and Rn to fit any requirement.

DELAY (Rp:Rn)	
1 : 0	144kΩ : 0Ω
1 : 0125	144kΩ : 18kΩ
1 : 1	144kΩ : 144kΩ
2 : 1	288kΩ : 144kΩ
0.076 : 1	11kΩ : 144kΩ