XC6132/33/34 High Performance Voltage Detectors

The XC6132/33/34 series are ultra-small voltage detectors that have high accuracy and sense pin for monitoring a rail other than VIN. High accuracy and a low supply current are achieved by means of a CMOS process, a high-accuracy reference power supply, and laser trimming technology.

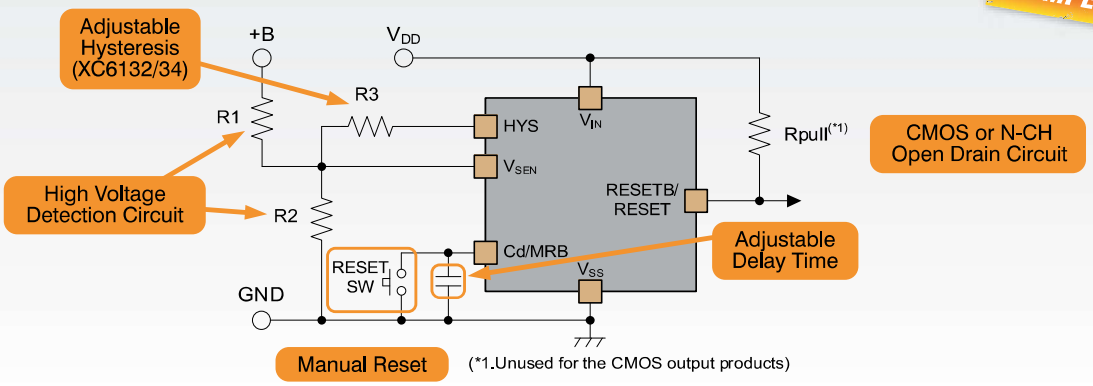
The sense pin is isolated from the power input pin to enable monitoring of the voltage of another power supply. Output can be maintained in the detection state even if the voltage of the power supply that is monitored drops to 0V. The sense pin is also suitable for detecting high voltages, and the detection and release voltage can be set as desired using an external resistance.

KEY FEATURES

SERIES	XC6132	XC6133	XC6134
Operating Voltage Range	1.6V ~ 6.0V	1.6V ~ 6.0V	1.6V ~ 6.0V
Detect Voltage Range	0.8V ~ 2.0V	1.0V ~ 5.0V	0.8V ~ 5.0V
Detect Voltage Accuracy	±1.2% (≥1.5V) ±18mV (<1.5V)	±1.5% (≥3.1V) ±1.2% (≥1.5V) ±18mV (<1.5V)	
Temp Characteristics	±50ppm/°C (typ)		
Output Configuration	CMOS or N-Channel Open Drain		
Output Logic	H level or L level at detection		
Power Consumption	1.28μA (VIN=1.6V) 1.36μA (VIN=6.0V)		
Hysteresis width	VDF×0.1% (typ)	VDF×5% (typ)	VDF×0.1% (typ)
Additional Features	ADJ Hysteresis Width	–	ADJ Hysteresis Width
	Manual RESET		
	Delay Capacitance Pin		
	Release delay/detection delay can be set 5 times ratio patterns		
	Sense Pin with Surge Voltage Protection	Sense Pin	
Op. Ambient Temperature	-40°C ~ +125°C		
Packages	USP-6C, SOT26		

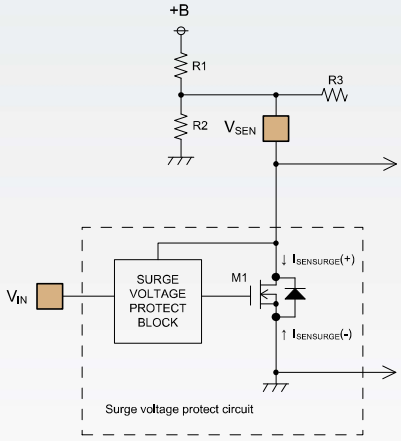
TYPICAL APPLICATION CIRCUIT

HIGH OPERATING TEMPERATURE



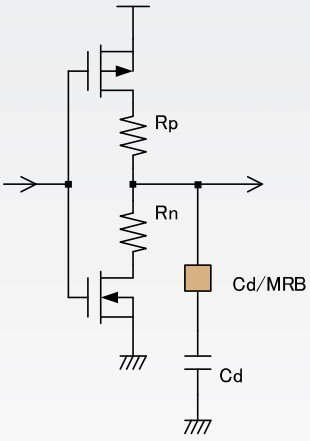
NEW FEATURES

XC6132 SURGE VOLTAGE PROTECTION



Even if 100V Load dump surge comes to +B, the internal surge voltage protection circuit protects the VSEN pin. When the surge comes and the VSEN voltage rises, the "SURGE VOLTAGE PROTECT BLOCK" detects it and turns on M1 which sinks 2.5mA and this current causes a voltage drop on R1 to keep VSEN safe.

RELEASE DELAY AND DETECTION DELAY COMBINATION



DELAY (Rp:Rn)	
1 : 0	144kΩ : 0Ω
1 : 0125	144kΩ : 18kΩ
1 : 1	144kΩ : 144kΩ
2 : 1	288kΩ : 144kΩ
0.076 : 1	11kΩ : 144kΩ

The release delay is set by Rp and Cd and the detect delay time is set by Rn and Cd. The release delay allows you to start up correctly and the detect delay avoids any mis-detection due to noise and spikes. The XC6132/33/34 has five (5) different ratio configurations of Rp and Rn to fit any requirement.

Automotive product qualification in accordance with AEC-Q100 (Grade 1)